What is Claimed is:

1. A serial bus controller using a nonvolatile ferroelectric memory, comprising:

a sense amplifier buffer unit for amplifying data applied from a plurality of cell array blocks;

a data bus unit for exchanging data between the plurality of cell array blocks and the sense amplifier buffer unit;

a data input/output buffer unit for buffering data inputted/outputted in the data bus unit;

a parallel/serial conversion controller for interconverting serial data inputted corresponding to serial clock signals with parallel data applied from the data input/output buffer unit; and

a write protecting controller for preventing data from being written in a corresponding sector of the plurality of cell array block when a write protecting command is set.

2. The serial bus controller according to claim 1, wherein the parallel/serial conversion controller comprises:

a counter for counting a corresponding address when

consecutive address/data are transmitted in a burst mode; and

a parallel/serial conversion unit for interconverting the serial data with the parallel data.

3. A serial bus controller using a nonvolatile ferroelectric memory, comprising:

a master for outputting serial data/address corresponding to serial clock signals into a serial bus;

a FRAM chip for controlling read/write operations of the memory depending on serial data/address and the serial clock signal received through the serial bus; and

a memory controller for controlling a response cycle of the serial clock signal depending on a code programmed in a nonvolatile ferroelectric memory to control access latency time differently according to kinds of address between the master and the FRAM chip.

4. The serial bus controller according to claim 3, wherein the memory controller comprises:

a nonvolatile latency program register for programming the code using the nonvolatile ferroelectric memory; and

a latency controller for outputting a control signal

to control the response cycle when interfacing is performed with the serial bus depending on a code programmed in the nonvolatile latency program register.

5. The serial bus controller according to claim 4, wherein the nonvolatile latency program register comprises:

a program command processor for outputting a command signal to code a program command in response to a write enable signal, a chip enable signal, an output enable signal and a reset signal;

a program register controller for performing a logic operation on input data, a power-up detecting signal and the command signal and outputting a write control signal and a cell plate signal;

a program register array for outputting a code signal programmed in a nonvolatile ferroelectric memory device in response to a pull-up enable signal, a pull-down enable signal, the write control signal and the cell plate signal; and

a reset circuit unit for outputting the reset signal into the program register controller in a power-up mode.

6. The serial bus controller according to claim 4, wherein the program command processor comprises:

a logic unit for performing a logic operation on the write enable signal, the chip enable signal, the output enable signal and the reset signal;

a flip-flop unit for sequentially flip-flopping the output enable signal corresponding to an output signal of the logic unit and outputting the command signal; and

an overtoggle detecting unit for detecting overtoggle of the output enable signal.

7. The serial bus controller according to claim 6, wherein the logic unit outputs the output enable signal when the chip enable signal and the write enable signal are at a low level, and enables the reset signal when one of the chip enable signal and the write enable signal transits to a high level.

8. The serial bus controller according to claim 7, wherein the logic unit comprises:

a first NOR gate for performing a NOR operation on the write enable signal and the chip enable signal;

a first AND gate for performing an AND operation on an output signal of the first NOR gate and the output enable signal; and

a second AND gate for performing an AND operation on

the output signal of the first NOR gate, the inverted reset signal and an output signal of the overtoggle detecting unit.

9. The serial bus controller according to claim 6, wherein the flip-flop unit comprises a plurality of flip-flops,

wherein the plurality of flip-flop units having data input nodes connected in series to data output nodes output the command signal from an output terminal of the last flip-flop, and flip-flop the output enable signal in response to an activation synchronizing signal applied from the logic unit.

10. The serial bus controller according to claim 9, wherein each of the plurality of flip-flops comprises:

a first transmission gate for selectively outputting an input signal depending on state of the activation synchronizing signal;

a first NAND gate for performing a NAND operation on an output signal of the first transmission gate and the reset signal;

a second transmission gate for selectively outputting an output signal of the first NAND gate depending on state

of the activation synchronization signal;

a third transmission gate for selectively outputting an output signal of the first transmission gate depending on state of the activation synchronizing signal;

a second NAND gate for performing a NAND operation on an output signal of the third transmission gate and the reset signal; and

a fourth transmission gate for selectively outputting an output signal of the second NAND gate depending on state of the activation synchronizing signal.

11. The serial bus controller according to claim 6, wherein the overtoggle detecting unit comprises a third NAND gate for performing a NAND operation on the command signal and the output enable signal.

12. The serial bus controller according to claim 5, wherein the program register controller comprises:

a third AND gate for performing an AND operation on the command signal and the input data;

a first delay unit for non-inverting and delaying an output signal of the third AND gate;

a second NOR gate for performing a NOR operation on output signals from the third AND gate and the first delay

unit;

a second delay unit for delaying an output signal of the second NOR gate and outputting the write control signal;

a third NOR gate for performing a NOR operation on an output signal of the second NOR gate and the power-up detecting signal; and

a third delay unit for non-inverting and delaying an output signal of the third NOR gate and outputting the cell plate signal.

13. The serial bus controller according to claim 5, wherein the program register array comprises:

a pull-up driver for pulling up a power voltage when the pull-up enable signal is enabled;

a first driver unit, cross-coupled to both terminals of a program register, for driving a voltage applied from the pull-up driver;

a write enable controller for outputting the reset signal and a set signal into both terminals of the program register in response to the write control signal;

a ferroelectric capacitor for generating voltage difference in both terminals of the program register in response to the cell plate signal;

a pull-down driver for pulling down a ground voltage when the pull-down enable signal is enabled; and

a second driving unit, cross-coupled to both terminals of the program register, for driving a voltage applied from the pull-down driver.

14. The serial bus controller according to claim 3, wherein the memory controller comprises:

a system controller for outputting a column address and a row address into the memory controller;

a bus for exchanging data, control signals and addresses between the memory controller and the system controller; and

a central control device for controlling the system controller.

15. The serial bus controller according to claim 3, wherein the FRAM chip comprises:

a sense amplifier buffer unit for amplifying data applied from a plurality of cell array blocks;

a data bus unit for exchanging data between the plurality of cell array blocks and the sense amplifier buffer unit;

a data input/output buffer unit for buffering data

inputted/outputted in the data bus unit;

a parallel/serial conversion controller for interconverting serial data inputted corresponding to serial clock signals with parallel data applied from the data input/output buffer unit; and

a write protecting controller for preventing data from being written in a corresponding sector of the plurality of cell array blocks when a write protecting command is set.

16. The serial bus controller according to claim 15, wherein the parallel/serial conversion controller comprises:

a counter for counting a corresponding address when consecutive address/data are transmitted in a burst mode; and

a parallel/serial conversion unit for interconverting the serial data with the parallel data.

17. A serial bus controller using a nonvolatile ferroelectric memory, comprising:

a memory controller for programming a code to control access latency time differently according to kinds of address in a nonvolatile ferroelectric memory and

outputting a response signal to confirm completion of transmission of serial data/address when the serial data/address are transmitted in response to serial clock signals received through a serial bus; and

a FRAM chip for performing read/write operations of the memory during a pulse interval of the response signal,

wherein the memory controller controls the pulse interval of the response signal with a first cycle when a row address is transmitted, and controls the pulse interval of the response signal with a second cycle shorter than the first cycle when a column address is transmitted.

18. The serial bus controller according to claim 17, wherein the memory controller controls the pulse interval of the response signal with the first cycle in a restore interval of the FRAM chip.

19. The serial bus controller according to claim 17, wherein the FRAM chip comprises:

a sense amplifier buffer unit for amplifying data applied from a plurality of cell array blocks;

a data bus unit for exchanging inter-data between the plurality of cell array blocks and the sense amplifier buffer unit;

a data input/output buffer unit for buffering data inputted/outputted in the data bus unit;

a parallel/serial conversion controller for interconverting serial data inputted corresponding to serial clock signals with parallel data applied from the data input/output buffer unit; and

a write protecting controller for preventing data from being written in a corresponding sector of the plurality of cell array blocks when a write protecting command is set.

20. The serial bus controller according to claim 19, wherein the parallel/serial conversion controller comprises:

a counter for counting a corresponding address when consecutive address/data are transmitted in a burst mode; and

a parallel/serial conversion unit for interconverting the serial data with the parallel data.